S.N.: 09/995,095
Art Unit: 2638

AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Listing of Claims:

1. (Original) A method for frame sync detection using signal combining and correlation, the method comprising the steps of:

despreading PN coded signals to provide in-phase I_1-I_n, and quadrature phase Q_1-Q_n signals, wherein each I_1-I_n and each Q_1-Q_n signal contains at least one sync bit and where $n \geq 2$;

summing the at least one sync bit from each I_1-I_n, and quadrature phase Q_1-Q_n signals to form sums I_{s1} and Q_{s1}, respectively;

providing a reference sync, wherein the reference sync comprises at least one bit;

comparing each sum I_{s1} and Q_{s1} with the at least one bit from the reference sync;

accumulating the results of each I_{s1} and Q_{s1} comparison so as to form two accumulates, I_A and Q_A, respectively;

squaring each accumulate I_A and Q_A, respectively, to form I_A^2 and Q_A^2;

summing I_A^2 and Q_A^2; and

comparing $I_A^2 + Q_A^2$ with a predetermined threshold and as a result of the comparison, making a determination whether frame sync has been achieved is made.

2. (Original) A method as in claim 1, wherein the step of despreading PN coded signals to provide in-phase I_1-I_n, and quadrature phase Q_1-Q_n signals further comprises the step of letting n=20.

3. (Original) A method as in claim 1, wherein the step of summing the at least one sync bit from each I_1-I_n and quadrature phase Q_1-Q_n signals to form sums I_{s1} and Q_{s1}, respectively, further comprises the step of forming sixteen sync bit sums from each I_1-I_n and quadrature phase Q_1-Q_n

signals.

4. (Original) A method as in claim 3, wherein the step of providing the reference sync further comprises the step of providing a sixteen-bit reference sync.

5. (Currently Amended) A method as in claim 1, wherein the step of providing the reference sync further comprises the step of storing the reference sync in a local accessible memory~~;~~.

6. (Original) A method as in claim 1, wherein the step of providing the reference sync further comprises the step of receiving the reference sync from a remote source.

7. (Original) A method as in claim 1, wherein the step of summing I_A^2 and Q_A^2 further comprises the steps of:

performing a square root operation on the sum $I_A^2 + Q_A^2$; and

comparing the square root of the sum $I_A^2 + Q_A^2$ with the predetermined threshold value.

8. (Original) A device for frame sync detection using channel combining and correlation, the device comprising:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1-In and, quadrature phase Q1-Qn channels, where $n \geq 2$;

at least one I-sync processor, wherein the I-sync processor is coupled to the channel despreader;

at least one Q-sync processor, wherein the Q-sync processor is coupled to the channel despreader;

an address controller coupled to the I-sync processor and the Q-sync processor;

a first summer connected to the I-sync processor and the Q-sync processor; and

a comparator, wherein the comparator is coupled to the first summer.

9. (Original) A device as in claim 8 wherein the channel despreader comprises a direct sequence spread spectrum (DSSS) despreader.

10. (Original) A device as in claim 8 wherein the channel despreader comprises a frequency hop

spread spectrum (FHSS) despreader.

11. (Currently Amended) A device as in claim 8 wherein the at least one I-sync processor comprises:

a first I-binary adder;

a first I-memory device, the first I-memory device coupled to the first I-binary adder;

a reference sync;

a first I-multiplier, wherein the first I-multiplier multiplies the reference sync with the output of the first I-memory device;

a first I-accumulator, wherein the first accumulator comprises:

a first I-register bank;

a second I-adder, the second I-adder having at least two inputs, wherein one of the two inputs is coupled to an output of the first I-register bank;

a second I-register bank, wherein an output of the second I-register bank is coupled to an input of the second I-adder; and

a first I-squaring device, wherein the first I-squaring device is coupled to the output of the second I-register ~~device~~ bank.

12. (Original) A device as in claim 11 wherein the first I-binary adder comprises a two's-complement adder.

13. (Original) A device as in claim 11 wherein the first I-memory device comprises a first dual port 16x16 RAM.

14. (Original) A device as in claim 8 wherein the at least one Q-sync processor comprises:

a first Q-binary adder;

a first Q-memory device, the first Q-memory device coupled to the first Q-binary adder;

a first Q-multiplier, wherein the first Q-multiplier multiplies the reference sync with the output of the first Q-memory device;

a first Q-accumulator, wherein the first Q-accumulator comprises:

a first Q-register bank;

a second Q-adder, the second Q-adder having at least two inputs, wherein one of the two inputs is coupled to an output of the first Q-register bank;

a second Q-register bank, wherein an output of the second Q-register bank is coupled to an input of the second Q-adder; and

a first Q-squaring device, wherein the first Q-squaring device is coupled to the output of the second Q-register device.

15. (Original) A device as in claim 14 wherein the first Q-binary adder comprises a two's-complement adder.

16. (Original) A device as in claim 14 wherein the first Q-memory device comprises a first dual port 16x16 RAM.

17. (Original) An integrated circuit (IC), wherein the integrated circuit comprises:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1-In and, quadrature phase Q1-Qn channels, where $n \geq 2$;

at least one I-sync processor, wherein the I-sync processor is coupled to the channel despreader;

at least one Q-sync processor, wherein the Q-sync processor is coupled to the channel despreader;

an address controller coupled to the I-sync processor and the Q-sync processor;

a first summer connected to the I-sync processor and the Q-sync processor; and

a comparator, wherein the comparator is coupled to the first summer.

18. (Original) An IC as in claim 17 wherein the IC comprises an Application Specific IC (ASIC).

19. (Original) An IC as in claim 17 wherein the IC comprises a field programmable gate array (FPGA).

20. (Original) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for frame sync detection using signal combining and correlation, the method comprising the steps of:

despreading PN coded signals to provide in-phase I_1-I_n, and quadrature phase Q_1-Q_n signals, wherein each I_1-I_n and each Q_1-Q_n signal contains at least one sync bit and where $n \geq 2$;

summing the at least one sync bit from each I_1-I_n, and quadrature phase Q_1-Q_n signals to form sums I_{s1} and Q_{s1}, respectively;

providing a reference sync, wherein the reference sync comprises at least one bit;

comparing each sum I_{s1} and Q_{s1} with the at least one bit from the reference sync;

accumulating the results of each I_{s1} and Q_{s1} comparison so as to form two accumulates, I_A and Q_A, respectively;

squaring each accumulate I_A and Q_A, respectively, to form I_A^2 and Q_A^2;

summing I_A^2 and Q_A^2; and

comparing $I_A^2 + Q_A^2$ with a predetermined threshold and as a result of the comparison, making a determination of whether frame sync has been achieved is made.

21. (Original) A program storage device as in claim 20 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

22. (New) A device as in claim 8 wherein the comparator compares a sum from the first summer with a predetermined threshold and, as a result of the comparison, a determination whether frame

sync has been achieved is made.

23. (New) A device as in claim 8 wherein the device provides non-coherent power detection.

24. (New) An integrated circuit as in claim 17 wherein the comparator compares a sum from the first summer with a predetermined threshold, and as a result of the comparison, a determination whether frame sync has been achieved is made.

25. (New) An integrated circuit as in claim 17 wherein the device provides non-coherent power detection.